LZ95G41

Single-chip Driver LSI for CCD

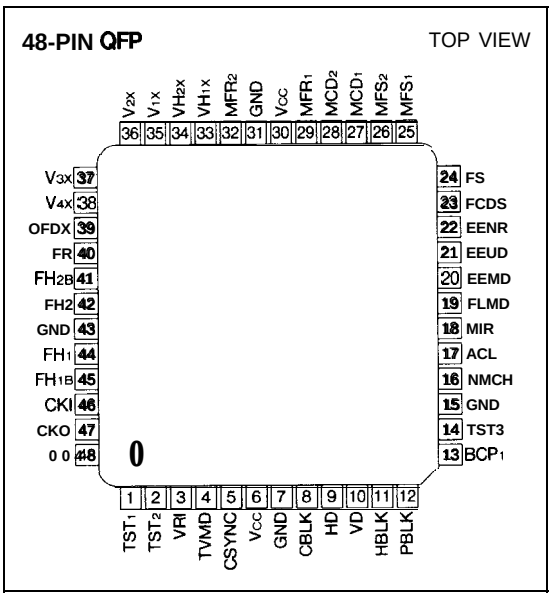
DESCRIPTION

The LZ95G41 is a CMOS single chip driver LSI which provides timing pulses used to drive a CCD area sensor, and generates synchronous pulses for TV signals and processing pulses for video signals.

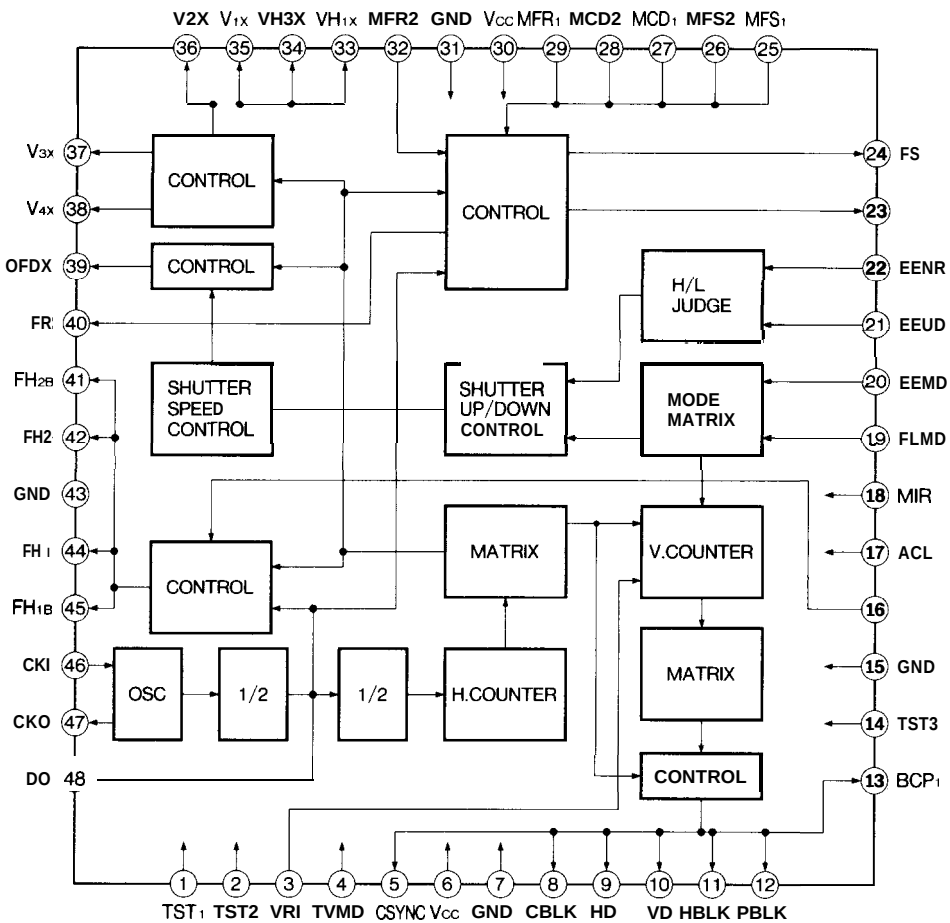
FEATURES

- Switchable between 270000 pixels B/W CCD and 320000 pixels B/W CCD
- Switchable between EIA and CCIR systems
- Built-in EE (Electronic Exposure) control (1/80 to 1/50000 s for EIA; 1/50 to 1/50 000 s for CCIR)
- Flicker-less function
- Switchable between normal and mirror image
- External synchronization is possible
- Single +5 V power supply
- Package : 48-pin QFP(QFP048-P-101 O)

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power voltage	Vcc	– 0.3 to + 7.0	v
Input voltage	VI	– 0.3 to Vcc +0.3	v
Output voltage	Vo	-0.3 to Vcc+0.3	v
Operating temperature	Topr	–30 to i-75	'c
Storage temperature	Tstg	–55 to +150	℃

DC CHARACTERISTICS

(Vcc = +5 V ± 10%, Ta=–30 to +75℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Low level input voltage	V_{IL}				1.5	v	1
High level input voltage	V_{IH}		3.5			v	
Low level output voltage	V_{OL1}	I_{OL} = 3.2 mA			0,4	v	2
High level output voltage	V_{OH1}	I_{OL} = – 1.6 mA	4.0			v	
Low level output voltage	V_{OL2}	I_{OL} =9.6 mA			0.4	v	3
High level output voltage	VOH2	I_{OH} = –4.8 mA	4.0			v	
Low level output voltage	V_{OL3}	I_{OL} = 4.8 mA			0.4	v	4
High level output voltage	V_{OH3}	I_{OH} = -2.4 mA	4.0			v	
Low level output current	$\|I_{IL1}\|$	VI=o v			1.0	μA	5
Low level output current	$\|I_{IL2}\|$	VI=o v	8.0		75	μA	6
High level output current	$\|I_{IH1}\|$	V_I = Vcc			1.0	μA	7
High level output current	$\|I_{IH2}\|$	VI= Vcc	8.0		75	μA	8

NOTES :

1. Applied to inputs (IC, ICU, ICD).
2. Applied to output (o).
3. Applied to output (O6M2).
4. Applied to output (O6M).
5. Applied to inputs (IC, ICD).
6. Applied to input (ICU).
7. Applied to inputs (IC, ICU).
8. Applied to input (ICD).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	TSTI	ICD	–	Test terminal 1	Testing pin. Typically connected to the GND level.
2	TST2	ICD	–	Test terminal 2	Testing pin. Typically connected to the GND level.
3	VRI	ICD	⌈	Vertical reset input	An input pin for resetting internal vertical, counter. The input pulse is necessary 1/2 horizontal max. delay from vertical synchronous start point, because VRI is counted by 2 times horizontal frequency. Set to H level when not resetting.
4	TVMD	ICD	–	TV mode select	An input pin to select TV standards. At EIA mode : H level At CCIR mode : L level
5	CSYNC	o	⌈	Composite shncronizing pulse	A composite synchronous signal.
6	Vcc	–	–	Power supply	Supply +5 V power.
7	GND	–	–	Ground	A grounding pin.
8	CBLK	o	⌐⌙	Composite blanking pulse	Composite blanking pulses.
9	HD	o	⌐⌙	Horizontal drive pulse	The pulse occurs at the start of lines.
10	VD	o	⌐	Vertical drive pulse	The pulse occurs at the start of every field.
11	HBLK	o	⌈	Horizontal blanking pulse	A pulse that corresponded to the cease period of the horizontal transfer pulse.
12	PBLK	o	⌐⌙	Pre-blanking pulse	Equivalent to CBLK (pin 8) pulse except for shorter pulse width with cut-off trailing edge.
13	BCPI	o	⌐⌙	Optical black clamp pulse	A pulse to clamp the optical black signal.
14	TST3	ICD	–	Test terminal 3	Testing pin. Typically connected to the GND level.
15	GND	–	–	Ground	A grounding pin.
16	NMCH	ICU	–	Horizontal transfer pulse 1 B, 2B control input	An input pin to select CCD area sensor. At mirror image CCD : H level At normal image CCD : L level
17	ACL	ICU	⌐	All clear input	An input pin to reset at power on, For details, see “NOTE 1”.
18	MIR	ICU	–	Mirror mode select	An input pin to switch CCD output. At mirror mode : H level At normal mode : L level
19	FLMD	ICU	–	Shutter control 1	For details, see “NOTES 2, 3“
20	EEMD	ICU	–	Electronic Exposure mode select	For details, see “NOTES 2, 3“’,

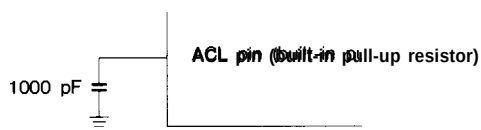
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
21	EEUD	IC	–	Electronic Exposure control 1	For details, see "NOTES 2, 3".
22	EENR	IC	–	Electronic Exposure control 2	For details, see "NOTES 2, 3".
23	FCDS	06M	⎍	CDS pulse 1	A pulse to clamp CCD output signals.
24	FS	06M	⎍	CDS pulse 2	A pulse to sampling CCD output signals.
25	MFSI	ICU	–	FS phase control 1	An input pin to control FS (pin 24) phase. For details, see "NOTE 4".
26	MFS2	ICU	–	FS phase control 2	
27	MCDI	ICU	–	FCDS phase control 1	An input pin to control FCDS (pin 23) phase. For details, see "NOTE 4".
28	MCD2	ICU	–	FCDS phase control 2	
29	MFRI	ICU	–	FR phase control 1	An input pin to control FR (pin 40) phase. For details, see "NOTE 4".
30	Vcc	–	–	Power supply	Supply +5 V power.
31	GND	–	–	Ground	A grounding pin.
32	MFR2	ICU	–	FR phase control 2	An input pin to control FR (pin 40) phase. For details, see "NOTE 4".
33	VH1X	o	⎍	Read out pulse	An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 1 BX pin of the LR36683N vertical driver LSI.
34	VH2X	0	⎍	Read out pulse	An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 3BX pin of the LR36683N vertical driver LSI.
35	VI x	0	⎍	Vertical transfer pulse 1	Vertical transfer pulse. To be connected to the 1 AX pin of the LR36663N vertical driver LSI.
36	V2X	0	⎍	Vertical transfer pulse 2	Vertical transfer pulse. To be connected to the 2AX pin of the LR36663N vertical driver LSI.
37	V3X	0	⎍	Vertical transfer pulse 3	Vertical transfer pulse. To be connected to the 3AX pin of the LR36663N vertical driver LSI.
38	V4X	0	u	Vertical transfer pulse 4	Vertical transfer pulse. To be connected to the 4AX pin of the LR36663N vertical driver LSI.
39	OFDX	0	⎍	OFD pulse output	An output pin to sweep the photodiode charge of CCD. When FLMD = EEMD = L, a pulse becomes H level signal.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
40	FR	06M2	⎍	Reset pulse	An output pulse to reset the CCD.
41	FH2S	06M2	⎎	Horizontal transfer pulse 2B	Horizontal transfer pulse. When MIR = L, the phase is the same as at FH_2. When MIR = H, the phase is the same as at FH_1.
42	FH2	06M2	⎍	Horizontal transfer pulse 2	Horizontal transfer pulse.
43	GND	–	–	Ground	A grounding pin
44	FH_1	06M2	⎍	Horizontal transfer pulse 1	Horizontal transfer pulse.
45	FH_{1B}	06M2	⎍	Horizontal transfer pulse 1 B	Horizontal transfer pulse. When MIR = L, the phase is the same as at FH_1. When MIR = H, the phase is the same as at FH_2.
46	CKI	ICK	⎍⎍	Clock input	A pin for oscillation inverter input, EIA : 1212 fH CCIR : 1236 fH (fH = Horizontal frequency)
47	CKO	OCK	⎎⎎	Clock output	A pin for oscillation inverter output.
48	DO	O	⎎⎎	Delay-live clock	I/2 frequency output of CKI (pin 46)

IC : Input pin (CMOS level)
ICU : Input pin (CMOS level with built-in pull-up resistor).
ICD : Input pin (CMOS level with built-in pull down resistor).
ICK : Input pin for oscillation.
OCK : Output pin for oscillation.
o : Output pin.
06M : Output pin.
06M2 : Output pin.

NOTES :

1. How to use ACL pin (Pin 17)



2. Fixed Shutter mode

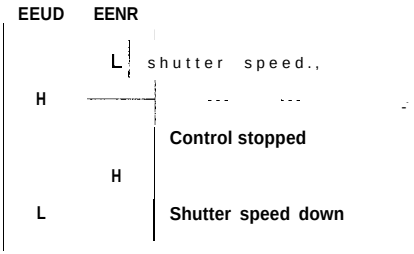
EEMD (Pin 20)= Low level

FLMD (Pin 19)	SHUTTER SPEED (s)	
	EIA	CUR
L	1 /60	1 /50
H	1/1 00 (Flicker-less)	

3. EE Control mode

EEMD (Pin 20)= Low level

FLMD (Pin 19)	SHUTTER SPEED (e)	
	EIA	CCIR
L	1 /60 to 1 /30 000	1 /50 to 1/m 000
H	1 /60 to 1 /50 000	1 /50 to 1 /50 000



- When EENR and EEUD are H level, control is stopped.
- When either EENR or EEUD is L level, control is resumed.

The shutter speed is changed in the table as shown below.

SHUTTER SPEED (S)	EIA	1/60 to 1/218	to 1 /556	to 1/1 100	to 1/2154
	CCIR	1/50 to 1/216	to 1 /552	to 1/1 092	to 1/2141
CHANGE STEP (S)	EIA	1/1 500	1/3900	1/7 800	1/15000
	CCIR	1/1 500	1/3 900	1/7 800	1/15000
SHUTTER SPEED (S)	EIA	to 1/3 656	to 1/12 070	to 1 /51 820	
	CCIR	to 1/3 836	to 1/12040	to 1 /52 460	
CHANGE STEP (S)	EIA	1 /31 000	1 /63 000	1/1 26000	
	CCIR	1 /31 000	1 /63 000	1/1 250~	

4. The phase adjustments should be made with the input combinations as shown in the table.

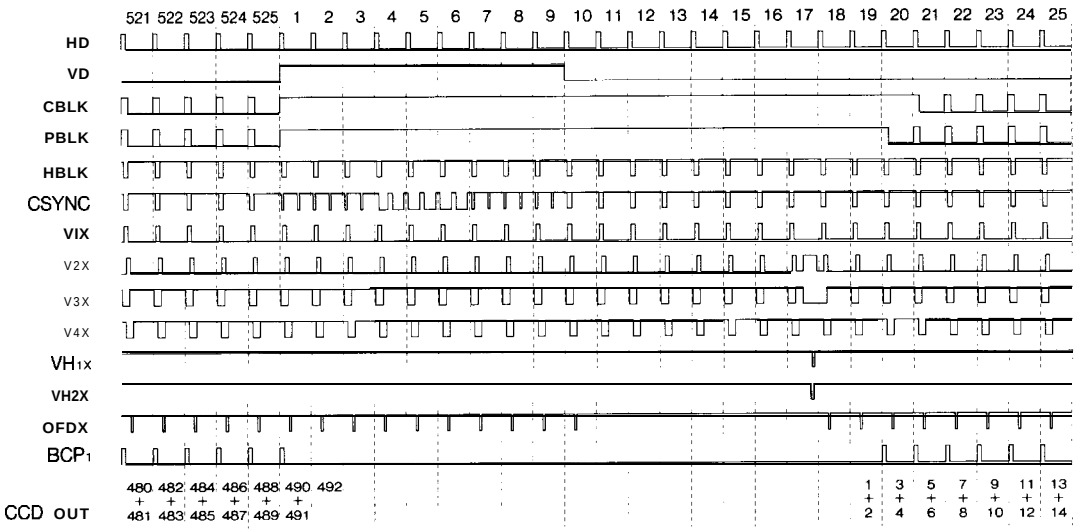
FS PHASE		FCD PHASE		FR PHASE		PHASE DELAY
MFS1	MFS2	MCD 1	MCD2	MFR 1	MFR2	(ns)
L	L	L	L	L	L	td
L	H	L	H	L	H	td + α
H	L	H	L	H	L	td + 2a
H	H	H	H	H	H	td + 3 α

TIMING DAIGRAM

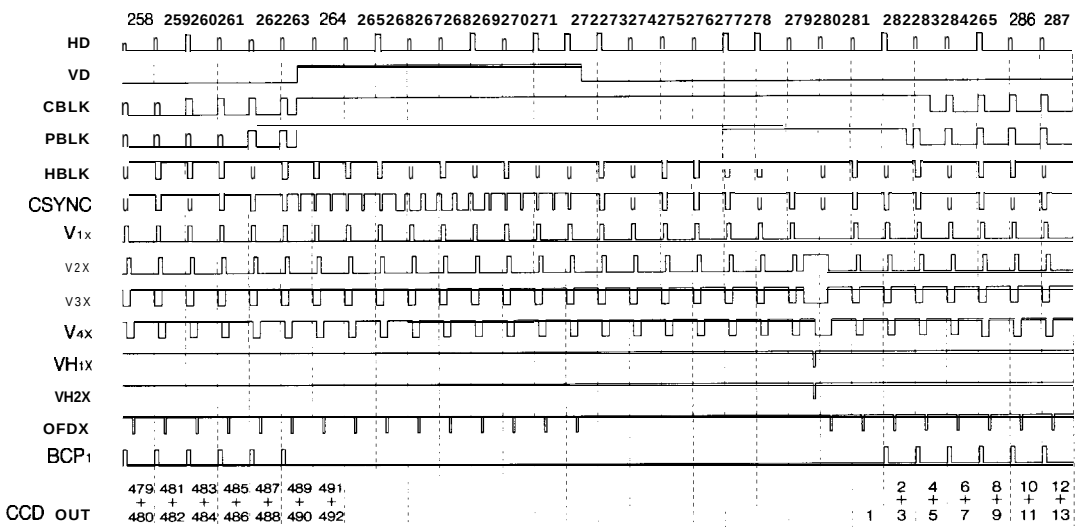
PULSE TIMING CHART < EIA >

Shutter speed 1/2000 s

(ODD FIELD)



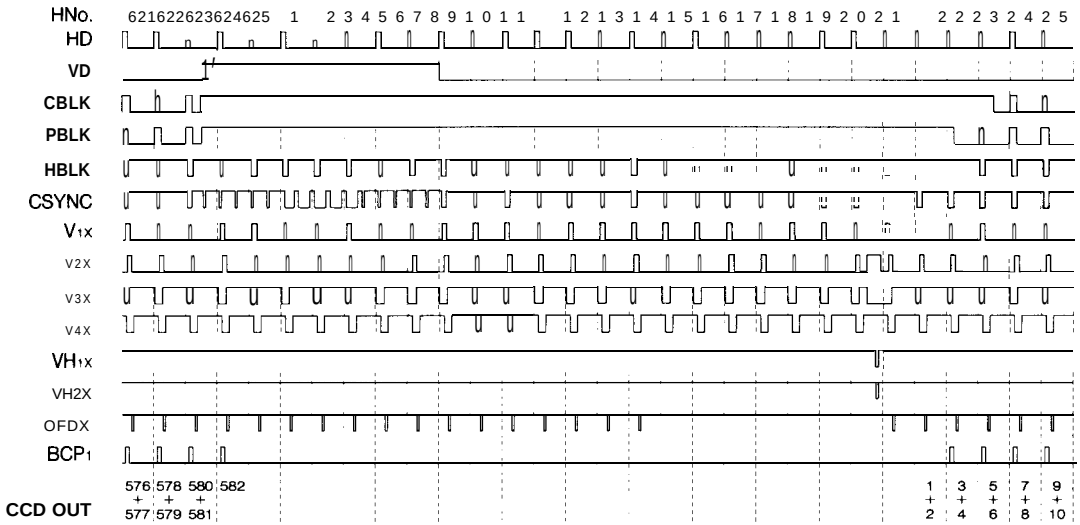
(EVEN FIELD)



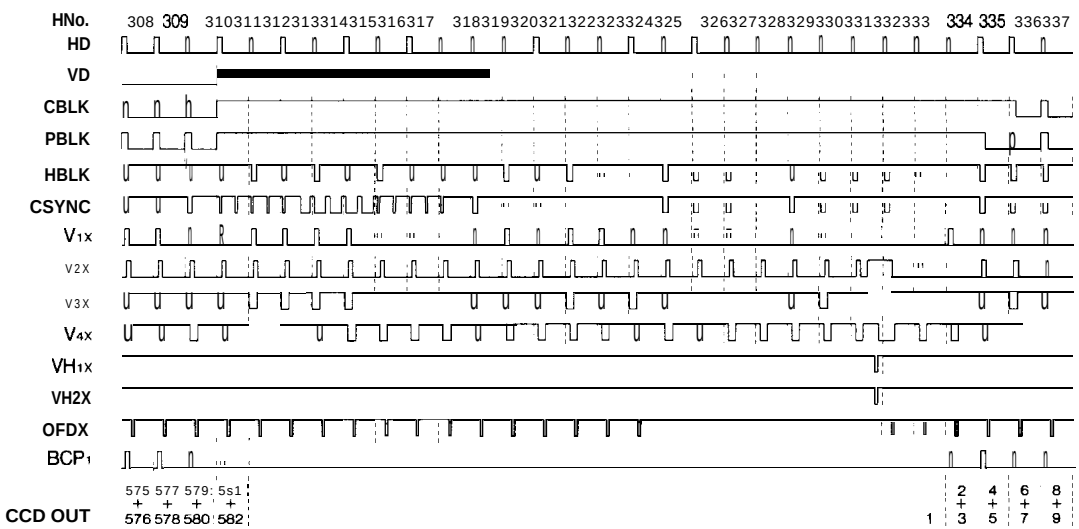
PULSE TIMING CHART <CCIR>

Shutter speed
1/2000 s

(1st, 3rd FIELD)

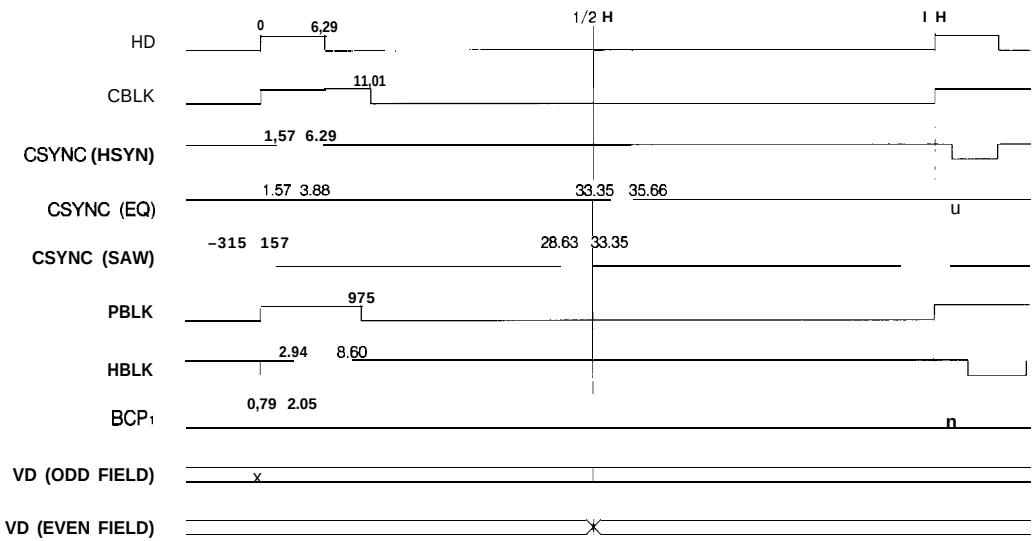


(2nd, 4th FIELD)

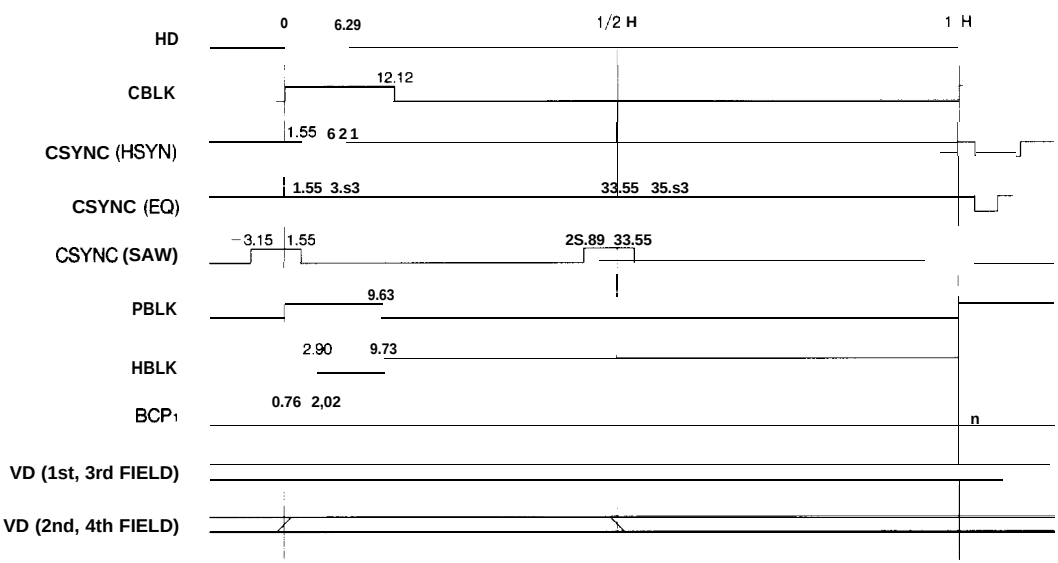


PULSE TIMING CHART <EIA>

Unit : μs

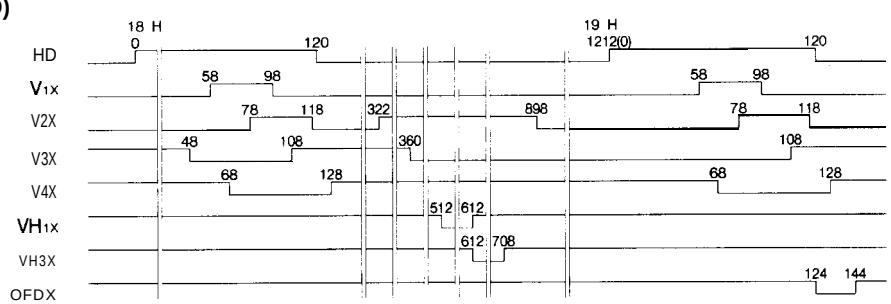


PULSE TIMING CHART <CCIR>

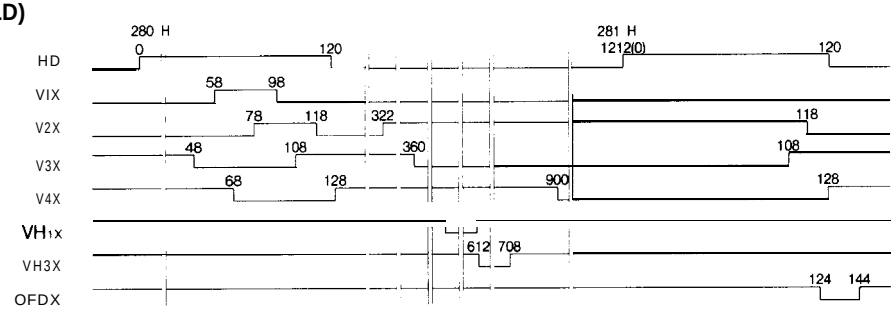


CHARGE READ TIMING < EIA, NORMAL (MIR = L) >

(ODD FIELD)

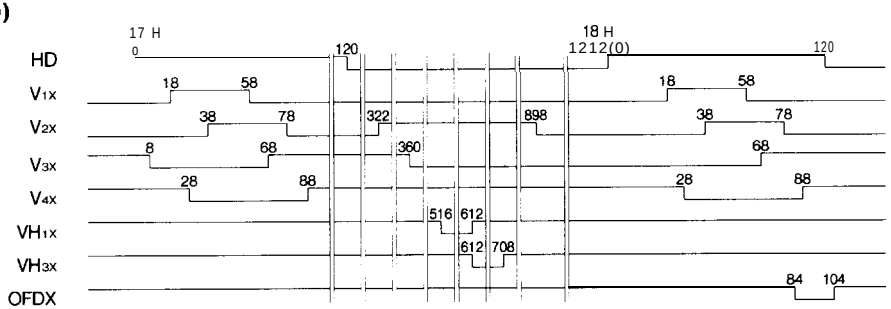


(EVEN FIELD)

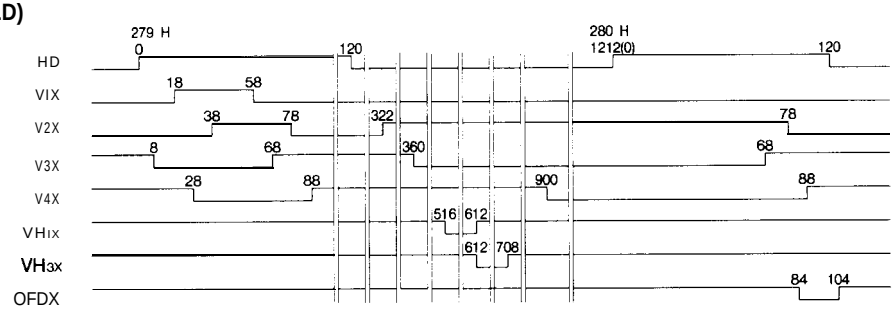


CHARGE READ TIMING < EIA, MIRROR (MIR =H) >

(ODD FIELD)

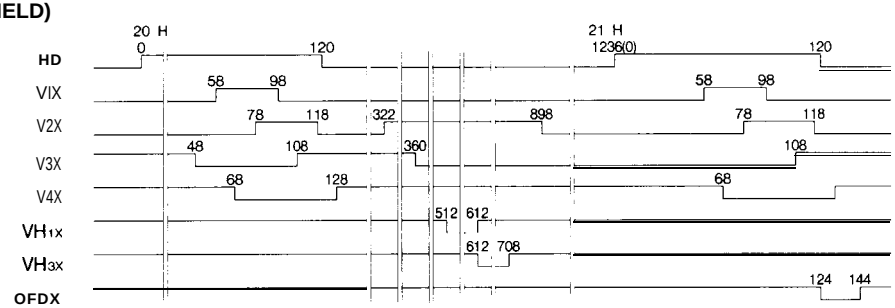


(EVEN FIELD)

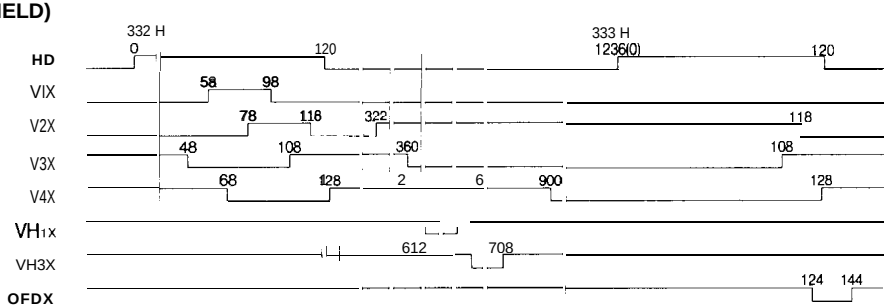


CHARGE READ TIMING <CCIR, NORMAL (MIR = L)>

(1st, 3rd HELD)

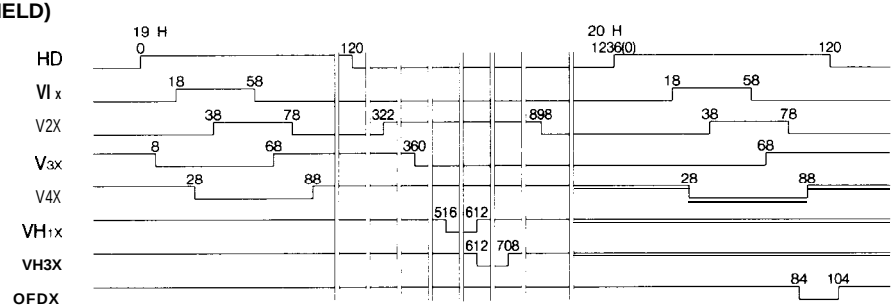


(2nd, 4th FIELD)

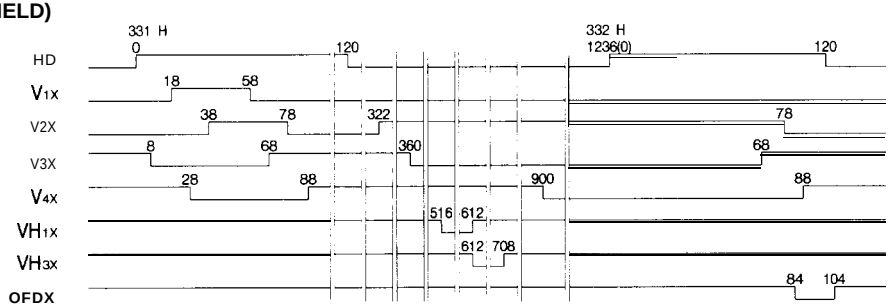


CHARGE READ TIMING <CCIR, MIRROR (MIR = H)>

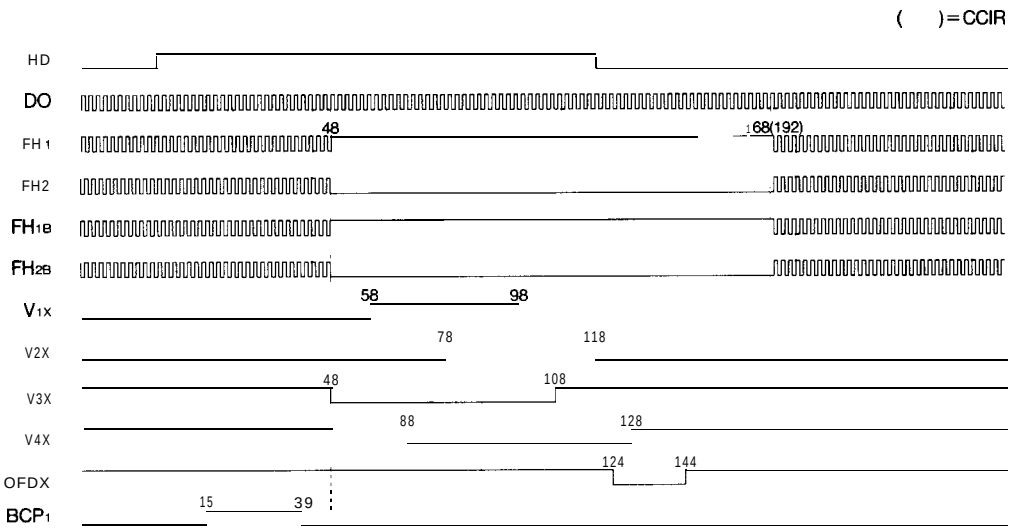
(1st, 3rd FIELD)



(2nd, 4th FIELD)



HIGH SPEED PULSE TIMING < NORMAL (MIR = L) >



HIGH SPEED PULSE TIMING < MIRROR (MIR = H) >